CLAIMS

What is claimed is:

1. A method for etching a feature with minimal RIE lag in an integrated circuit wafer incorporating at least one layer of organosilicate glass dielectric, the method comprising:

positioning the wafer in a reaction chamber;

introducing a flow of etchant gas mixture including C4F8 and CF4 into the reaction chamber; and

striking a plasma with the etchant gas in the reaction chamber.